LISTING OF CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application.

Claims 1-13 (Canceled)

Claim 14 (Currently Amended): A semiconductor device comprising:

a semiconductor substrate;

a first impurity diffusion layer formed in the semiconductor substrate;

a second impurity diffusion layer formed in the semiconductor substrate in a spaced-apart relation to the first impurity diffusion layer;

a first insulating layer formed on the first impurity diffusion layer so as to cover the first impurity diffusion layer except for a tip portion opposite to the second impurity diffusion layer;

a second insulating layer formed on the second impurity diffusion layer so as to cover the second impurity diffusion layer except for a tip portion opposite to the first impurity diffusion layer;

a trench formed over the semiconductor substrate in a manner to be defined between the first insulting layer and the second insulating layer;

a gate insulating film lined on a bottom surface and an inner sidewall surface of the trench; and

a gate electrode formed as a conductive layer in the trench with the gate insulting film intervening between the gate electrode conductive layer and the trench, the gate electrode

conductive layer being formed in an overlapped relation relative to the tip portion of the first impurity diffusion layer and the tip portion of the second impurity diffusion layer,

wherein the gate insulating film contains one selected from the group consisting of Ta_2O5, Al_2O_3, $BaSrTiO_3$, Zr oxide Hf oxide, Sc oxide, Y oxide, and Ti oxide.

Claim 15 (Currently Amended): The semiconductor device according to claim 14, wherein the gate insulating film is formed of an ~~insulting~~ insulating material having a dielectric constant of above 5.

Claim 16 (Canceled)

Claim 17 (Currently Amended): The semiconductor device according to claim 14, wherein the first impurity diffusion layer and the second impurity diffusion layer, each, comprise a third impurity diffusion layer forming a corresponding tip ~~including~~ portion ~~formed~~ beneath the gate insulating film formed on the inner sidewall surface of the trench and a fourth impurity diffusion layer including a portion formed beneath ~~any of~~ a corresponding one of the first insulating layer and second insulating layer and having a deeper junction in the semiconductor substrate than the third impurity diffusion layer.

Claim 18 (Currently Amended): The semiconductor device according to claim 14, further comprising a metal silicide layer formed on the first impurity diffusion layer and the

second impurity diffusion layer at those areas ~~beneath~~ adjacent to the first insulating layer and the second insulating layer.

Claim 19 (Canceled)